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Applicant

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Abstract

A memory controller (42) supports a mode know as continuous page mode. The memory controller (42) is coupled to a pipelined internal bus and provides control signals to an external bus to control a memory such as a dynamic random access memory (DRAM) (43). The memory controller (42) compares the page portion of a next address to the page portion of the current address. If the addresses match, the memory controller (42) keeps the page open for the next cycle. However if the addresses do not match, or if the next address is not valid at this same point in time during the first access, the memory controller (42) closes the page during the first cycle. The memory controller (42) performs continuous page mode without incurring a penalty when the page is closed.